REMARKS

I. Introduction

With the cancellation herein without prejudice of claims 8 to 15 and addition of new claims 16 to 135, claims 16 to 135 are currently pending in the present application. In view of the foregoing amendments and following remarks, it is respectfully submitted that all of the presently pending claims are allowable, and reconsideration is respectfully requested.

Applicants note with appreciation the acknowledgement of the claim for foreign priority and the indication that all of the certified copies of the priority documents have been received.

Applicants thank the Examiner for considering the previously filed Information Disclosure Statement, PTO-1449 papers, and cited references.

II. Rejection of Claims 8 and 15 Under 35 U.S.C. § 101

While Applicants do not agree with the merits of this rejection, claims 8 to 15 have been canceled herein without prejudice, thereby rendering moot the present rejection.

III. Rejection of Claims 8 to 15 Under 35 U.S.C. § 102(b)

Claims 8 to 15 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. Patent No. 6,052,773 ("DeHon et al.").

While Applicants do not necessarily agree with the merits of this rejection, claims 8 to15 have been canceled herein without prejudice, thereby rendering moot the present rejection.

IV. New Claims 16 to 135

Claims 16 to 135 have been added herein. New claims 16 to 135 do not add any new matter and are fully supported by the present application, including the Specification.

It is respectfully submitted that DeHon et al. do not render unpatentable the present claims for at least the following reasons.

Data processing today relies largely on sequential processors such as the INTEL-Pentium-architecture. The sequential way of data processing is becoming more and more inadequate for processing streams of data, for example audio streams and video streams, where the same operation has to be executed over and over again with new data samples.

For processing data streams, arrays including a plurality of data cells such as FPGAs and the like are suited much better. However, an array for processing data is not as suited for sequential tasks as is the sequential processor per se.

In order to obtain the best of both worlds, both architectures may be coupled to each other. However, the coupling strongly influences overall performance of the architecture.

It has been suggested in the prior art that a strict coupling is highly preferable and that that attaching reconfigurable logic to the memory bus of any other kind of processor external bus should be avoided. It has also been suggested in the prior art that any kind of interfacing scheme that attaches reconfigurable resources to a slow bus operating asynchronously or at a lower clocking frequency than the internal data path of the processor will always be a bottleneck.

The features recited in the present claims provide improved couplings not disclosed or suggested in the prior art.

Independent claim 16, for example, relates to a data processing arrangement, and recites, inter alia, the following:

> *. . . an instruction pipeline including a FIFO . . . said FIFO is arranged for storing at least some of the at least one of configuration load instructions and configuration preload instructions in a manner that makes them available to be fed from the FIFO to the reconfigurable array, the feeding effecting at least one of loading and preloading of configuration data, the configuration data defining how data processing is to proceed.*

Thus, the array is coupled to the instruction pipeline such that configurations can be loaded from a FIFO. Accordingly, a very loose coupling is provided where the sequential processor that usually represents the host for the data processing array need not transfer every single configuration bit into the array. Instead, only a configuration load instruction is to be transferred to the array. Therefore, the coupling is very loose.

Applicant has surprisingly found that, a loose coupling using configuration load instructions for loading configuration data, as provided for in the context of claim 16, does not reduce performance as expected but actually enhances the performance by making it possible to have an asynchronous way of data processing between the two units while still allowing for data streaming.

DeHon et al., does not disclose or suggest these features, so that claims 16 and its dependent claims 17 to 41 are allowable.

Independent claim 42, relates to a data processing method, and recites, inter alia, the following:

> *. . . providing an instruction pipeline that pipelines instructions and that couples a reconfigurable array to the at least one standard processor as a virtual processor in a Simultaneous Multithreading (SMT) environment . . .*

DeHon et al. do not disclose or suggest such a coupling or an instruction pipeline that provides the coupling as provided for in the context of claim 42. Thus, DeHon et al. do not disclose or suggest all of the features of claim 42, so that claim 42 and its dependent claims 43 to 56 are allowable.

Independent claim 57, relates to a data processing method, and recites, inter alia, the following:

> *. . . providing a reconfigurable array of data processing cells for data processing [the array coupled to a standard processor via an instruction pipeline]; . . . and coupling the reconfigurable array to a memory hierarchy via an explicitly software managed cache . . .*

DeHon et al. do not disclose or suggest such a coupling of a reconfigurable array to a memory hierarchy as provided for in the context of claim 57. Thus, DeHon et al. do not disclose or suggest all of the features of claim 57, so that claim 57 and its dependent claims 58 to 74 are allowable.

Independent claim 75, relates to a data processing arrangement, and recites, inter alia, the following:

> *. . . a reconfigurable array including a plurality of data processing cells coupled to the at least one standard processor via the instruction pipeline; and a plurality of IRAM memory elements coupled to the reconfigurable array, at least some of the IRAM memory elements adapted for storing local cache copies of a main memory.*

DeHon et al. do not disclose or suggest such a coupling of a IRAM memory elements to a reconfigurable array as provided for in the context of claim 75. Thus, DeHon et al. do not disclose or suggest all of the features of claim 75, so that claim 75 and its dependent claims 76 to 91 are allowable.

Independent claim 92, relates to a data processing arrangement, and recites, inter alia, the following:

> *. . . providing at least one standard processor for processing data in a sequential manner, the at least one standard processor including an instruction pipeline via which the reconfigurable array is coupled to the at least one standard processor; and coupling the reconfigurable array to a cache, which is explicitly software managed to contain local cache copies of a main memory, the cache including a plurality of IRAM memory elements.*

DeHon et al. do not disclose or suggest such a coupling of an array to a cache, which is explicitly software managed as provided for in the context of claim 92. Thus, DeHon et al. do not disclose or suggest all of the features of claim 92, so that claim 92 and its dependent claims 93 to 106 are allowable.

Independent claim 107, relates to a data processing method, and recites, inter alia, the following:

> *. . . providing at least one standard processor for processing data in a sequential manner, the at least one standard processor including an instruction pipeline via which the reconfigurable array is coupled to the at least one standard processor; and coupling the reconfigurable array to a de-centralized explicitly preloaded configuration cache, wherein the cache is adapted for being fed instructions for the reconfigurable array by the at least one standard processor.*

DeHon et al. do not disclose or suggest coupling a reconfigurable array to a de-centralized explicitly preloaded configuration cache, wherein the cache is adapted for being fed instructions for the reconfigurable array by at least one standard processor as provided for in the context of claim 107. Thus, DeHon et al. do not disclose or suggest all of the features of claim 107, so that claim 107 and its dependent claims 108 to 120 are allowable.

Independent claim 121, relates to a data processing method, and recites, inter alia, the following:

> *. . . providing at least one standard processor for processing data in a sequential manner, the at least one standard processor including an instruction pipeline via which the reconfigurable array is coupled to the at least one standard processor; coupling the reconfigurable array to a cache for data processing, the cache containing local cache copies of a main memory, including a plurality of IRAM memory elements, and being explicitly software managed; and coupling the reconfigurable array to a de-centralized explicitly preloaded configuration cache, thereby supporting preloading of at least one of a configuration and a fast configuration switch.*

DeHon et al. do not disclose or suggest coupling the reconfigurable array to cache for data processing, the cache containing local cache copies of a main memory, and do not disclose or suggest coupling a reconfigurable array to a de-centralized explicitly preloaded configuration cache, wherein the cache is adapted for being fed instructions for the reconfigurable array by at least one standard processor, as provided for in the context of claim 121. Thus, DeHon et al. do not disclose or suggest all of the features of claim 121, so that claim 121 and its dependent claims 122 to 135 are allowable.

V. Conclusion

In light of the foregoing, it is respectfully submitted that all of the presently pending claims are in condition for allowance. Prompt reconsideration and allowance of the present application are therefore earnestly solicited.

Respectfully submitted,

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